

Fabrication of 20 nm embedded longitudinal nanochannels transferred from metal nanowire patterns

Category: (3) Fabrication Technology

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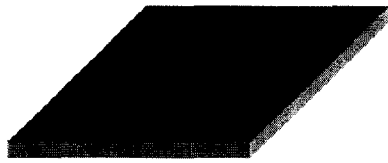
Novelty: In this abstract we describe a technique for fabricating nanometer-scale channels embedded by dielectric materials. Longitudinal “embedded” nanochannels with an opening size 20 nm x 80 nm have been successfully fabricated on silicon wafer by transferring sacrificial nanowire structures.

Background: The traditional electron beam lithography and more recently developed focused ion beam (FIB) milling/lithography techniques have been exploited for generating *exposed* nanometer-size nanochannels for the manipulation and analysis of biomolecules such as DNA and proteins at single molecule resolution [1]. An additional process step of sealing exposed nanochannels can’t be avoided to generate complete nanodevices. Currently, sealing techniques such as wafer bonding and soft elastomer sealing are being used for sealing micrometer-scale exposed channels. However, current wafer bonding requires defect free and flat surface, and elastomer sealing process comes with clogging because of soft material intrusion into the channels [2]. Our proposed technique provides a wafer bonding-free process to fabricate embedded nanochannels.

Fabrication Process: Longitudinal nanometer-scale embedded channels have been fabricated by a sacrificial nanowire etching technique. In our fabrication, an array of nanometer-scale metal nanowire patterns was first fabricated on SiO₂/silicon wafer using Focused Ion Beam (FIB) lithography and a subsequent metalization/lift-off process. The metal nanowire patterns were transferred onto SiO₂ layer by reactive ion etching (RIE). Figure 1 shows the SiO₂ nanowire prepared by FIB lithography and a subsequent RIE process. Nanometer-scale SiO₂ nanowires as sacrificial patterns were obtained after removing metal mask patterns (Fig. 2-a). Plasma Enhanced Chemical Vapor Deposition (PECVD)dielectrics were deposited on the SiO₂ nanowire patterns (Fig 2-b). FIB milling was used to generate trenches both front region and rear region of the nanowires (Fig. 2-c). Figure 3 shows a cross-sectional view of the 20 nm x 80 nm size SiO₂ nanowire patterns embedded by PECVD dielectrics. Those trenches provided openings through which etchant chemicals (BOE) were going. As a result of a different etch rate of SiO₂ and dielectrics in BOE, “embedded” nanochannel patterns were fabricated on silicon substrates (Fig. 2-d). In order to reveal that channels were gone through two openings, FIB milling was used for a fast and precise analysis. Figure 4-a shows the big trenches prepared by FIB milling for generating openings for easy sacrificial etching and the small trenches for etching analysis. The 20 nm x 80 nm x 3 μm long enclosed channel is shown in Figure 4-b. Five various lengths (3, 6, 8, 10, 20 μm) of pillar patterns were tried to find a maximum length of enclosed channels which were able to be generated without experiencing “diffusion-blocking” during a sacrificial pillar etching process. 3 μm long longitudinal nanochannels were successfully fabricated.

References:

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2. M. Stjernstrom and J. Roerrade, J. Micromech. Microeng. 8, 33, 1998.
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(a) Fabricate SiO_2 nanowires by FIB lithography and a subsequent RIE

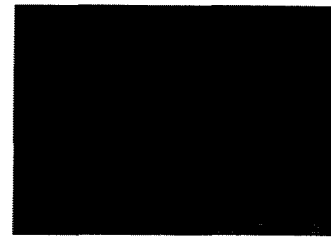
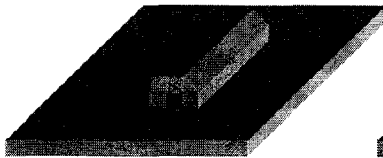


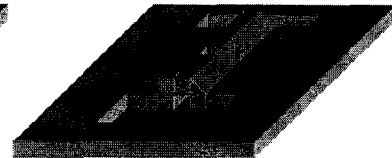
Fig.1 Scanning electron micrograph showing nanometer-scale SiO_2 nanowire prepared by FIB lithography and a subsequent RIE process. The metal mask still remained on the top of the nanowire.



(b) Deposit PECVD dielectrics



(c) Generate trenches by FIB milling



(d) Etch sacrificial nanowires by BOE

Fig.2 Fabrication process of enclosed nanochannels. (a) fabricating SiO_2 nanowires (b) depositing PECVD dielectrics (c) generating trenches by FIB (d) etching sacrificial nanowires by BOE.

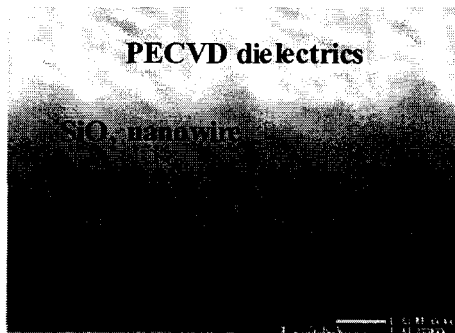
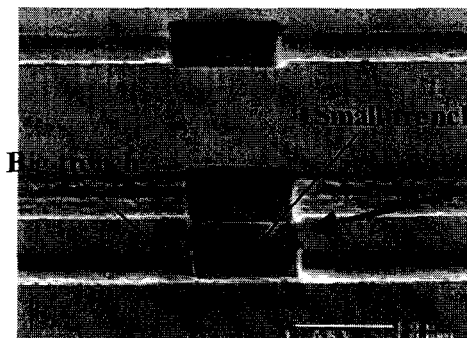
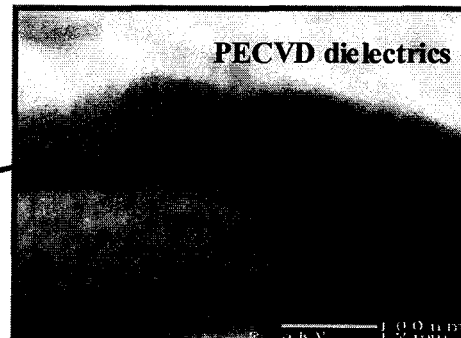


Fig. 3 Scanning electron micrograph showing a cross sectional view of sacrificial SiO_2 nanowires embedded by PECVD dielectric layers.



(a)



(b)

Fig. 4 (a) Scanning electron micrograph showing a big trench prepared by FIB for generating openings for easy sacrificial etching and a small trench for a fast and precise etch analysis. (b) scanning electron micrograph indicating a cross sectional view of 20 nm x 80 nm enclosed nanochannels.